Remarks

Reconsideration of the application as amended herein is respectfully requested. Claims 1-4 are pending in this application. Claim 1 has been amended. No claims have been added or cancelled.

Claim Rejections – 35 U.S.C. §103

The Office Action has rejected claims 1-4 under 35 U.S.C. § 103(a) as being unpatentable over Beausoleil et al., U.S. Patent No. 5,551,013 (hereinafter "Beausoleil") in view of Austin et al., U.S. Patent No. 4,885,684 (hereinafter "Austin") and further in view of Baker et al., U.S. Patent No. 5,701,502 (hereinafter "Baker"). Applicants respectfully traverse this rejection.

"To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." MPEP 2143. As explained below, Beausoleil, Austin, and Baker, either alone or in combination, fail to teach or suggest all of the limitations of Claim 1. Furthermore, there is no suggestion or motivation combine these references.

The Cited References Do Not Teach Or Suggest All Of The Claim Limitations

The 5/20/05 Office Action states:

> [T]he whole phrase as claimed entails that one processor is allowed to effect data between the main memory, not the rest of the processors which are being emulated in a particular emulation code execution state. . . . As construed by the claim, a maintenance bus is present in the course of states of emulation, a bit detected so to allow only just one processor to access a shared memory while preventing all target processors from accessing it. Such bit event is interpreted as a dynamic maintenance adjustment being triggered via a code to allow memory to be modified by just one processing unit with the rest of the system being kept off; and this is

> reminiscent of synchronization of shared memory by one memory processor in an exclusive session – and this synchronization process was a known concept, the detection of which control code dictates that one and only one processor can modify the content of such shared memory.

See 5/20/05 Office Action at 8-9. In short, the Office Action has broadly interpreted the term "work station" to mean a module processor located within a module and capable of being emulated in a particular emulation code execution state.

Claim 1 has been amended to recite that the work station is "**external** to the plurality of modules." (emphasis added). Claim 1, as amended, also recites "transferring **external** data between said work station and said module main memory" and "allowing **external** data to be transferred between said work station and said module main memory during the in progress emulation." (emphasis added). Support for the amendments can be found on page 6, lines 22-24 of the Application. Beausoleil, Austin and Baker, either alone or in combination, do not teach or suggest all of the limitations of Claim 1 as amended.

Moreover, Baker discloses fault-tolerant hardware synchronization. Specifically, Baker discloses:

> One of the more unique and significant features of the S/88-S/370 processing units is the self-determined synchronization of any processing unit such as 21 by a currently-processing partner 23. The S/88 entity of each unit has the capability and the responsibility for the synchronization of a new or error producing partner. When a S/88 entity of a unit assumes this responsibility, it is referred to as the "master." Its partner, which undergoes synchronization, is referred to as the "slave." . . . [A]ny time the S/88 determines that a S/88 (slave) entity requires synchronization with its partner (master), that synchronization is permitted to progress to a suitable point after the S/88 slave entity has been "kicked-off"; then the execution is diverted to the corresponding S/370 entity. . . . The S/88 entities of all processing units detect and process the interrupt with each assuming it is a slave until a default master is established. That master then kicks off any holding slave in lock step, each resuming the pre-empted environment of the master (upon returning from the interrupt).

See Baker, Col. 118, Line 49 to Col. 119, Line 18. In other words, Baker discloses that a processing unit is able to "kick off" its partner processing unit during an interruption in order to synchronize with the partner processing unit. Nevertheless, Baker fails to disclose or suggest that data transfers between a module's main memory and the module's processors are blocked

and that **external** data is allowed to be transferred between the module's main memory and a work station located **external** to the module.

In addition, neither Beausoleil nor Austin discloses or suggests that data transfers between a module's main memory and the module's processors are blocked and that **external** data is allowed to be transferred between the module's main memory and a work station located **external** to the module. Beausoleil merely discloses a MOP bit that controls whether a module processor will emulate a logic function or a memory function. *See Beausoleil*, Col. 6, Lines 14-27. Austin merely discloses a maintenance bus. *See Austin*, Col. 6, Lines 4-26. At best, the combination of Beausoleil, Austin, and Baker only discloses or suggests a bit that denies access of a memory to module processors located on a module except for one module processor. But the combination of Beausoleil, Austin, and Baker fails to teach or suggest "a work station external to the plurality of modules" and a block code that "blocks data transfers between said plurality of module processors and said module main memory during the emulation step that includes the blocking code thereby allowing external data to be transferred between said work station and said module main memory during the in progress emulation," as recited in Claim 1. Accordingly, Claim 1, as amended, is allowable over the cited references.

There Is No Motivation Or Suggestion To Combine The References

Like the present invention, Beausoleil relates to the emulation of integrated circuit designs. Austin and Baker, however, relate to completely different and unrelated technologies. Austin relates to a distributed data processing network, which has nothing to do with the emulation of integrated circuit designs. *See, e.g., Austin*, Cols. 1-3. Similarly, Baker relates fault-tolerant mainframe computer systems, which has nothing to do with the emulation of integrated circuit designs. *See, e.g., Baker*, Col. 7, Lines 33-38 ("Accordingly, it is intended that the present improvement will provide a fault tolerant environment and architecture for a normally non-fault-tolerant processing system and operating system without major rewrite of the operating system. In the preferred embodiment a model of IBM System/88 is coupled to a model of an IBM S/370.").

There is simply no suggestion or motivation in any of these references to combine the references with one another. *See* MPEP 2143. "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oetiker*, 977 F.2d 1443, 1446 (Fed. Cir. 1992). One of ordinary skill in the art would not look to combine Austin or Baker with Beausoleil. Not only do these references relate to different areas of technology, they were not directed "to precisely the same problem of underpinning slumping foundations." *Ruiz v. A.B. Chance Co.*, 357 F.3d 1270, 1276 (Fed. Cir. 2004). For example, Beausoleil sought to address "the slowness of test execution and the difficulty and cost of generating and running a complete suite of test cases" for software simulation of a VLSI chip design. *See Beausoleil*, Col. 1, Line 65 to Col. 2, Line 3. Austin sought to address "the problem of distributing the overall complex function to be performed between the plurality of processors." *See Austin*, Col. 1, Line 68 to Col. 2, Line 2. Baker sought to improve the "means for permitting a central processing unit (CPU) of a data processing system to interact with apparatus which is alien to the operating system under which the data processing system is operating." *See Baker*, Col. 3, Lines 42-45. Thus, neither Austin nor Baker is directed to the same problem sought to be addressed by Beausoleil, and each is not reasonably pertinent to the particular problem sought to be addressed by Claim 1.

Dependent Claims 2-4

The foregoing arguments apply to Claims 2-4, as they all are dependent on Claim 1. Therefore, Applicants respectfully submit that Claims 2-4 are allowable as well.

Conclusion

For the foregoing reasons, the Office Action has failed to establish a prima facie case of obviousness under 35 U.S.C. § 103. *See* MPEP 2143. Therefore, Applicants respectfully submit that this application is in condition for allowance, which is respectfully requested. Should the Examiner have any questions or comments on the application, the Examiner should feel free to contact the undersigned via telephone.

The Commissioner is authorized to charge any fee which may be required in connection with this Amendment to deposit account No. 15-0665.

Respectfully submitted,

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Dated: August 17, 2005

By: _____

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